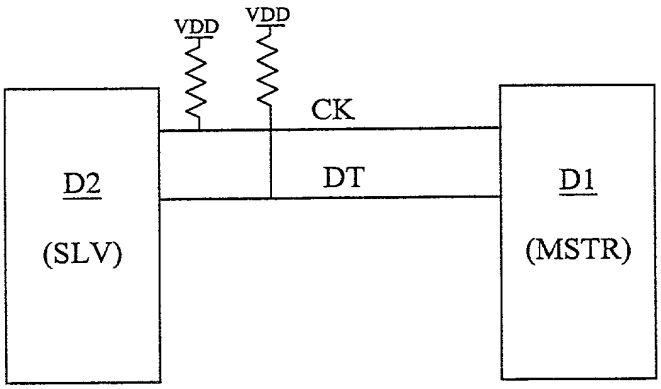


FIG. 1

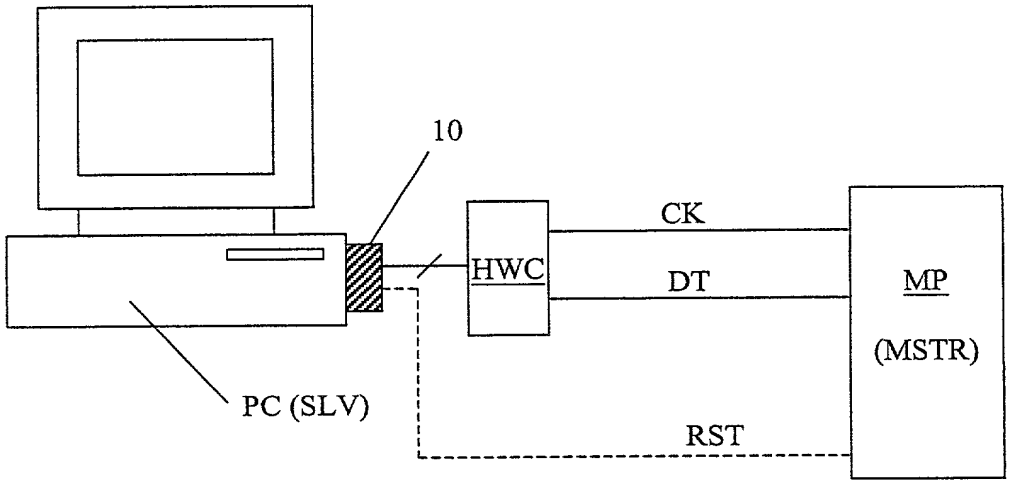


FIG. 7

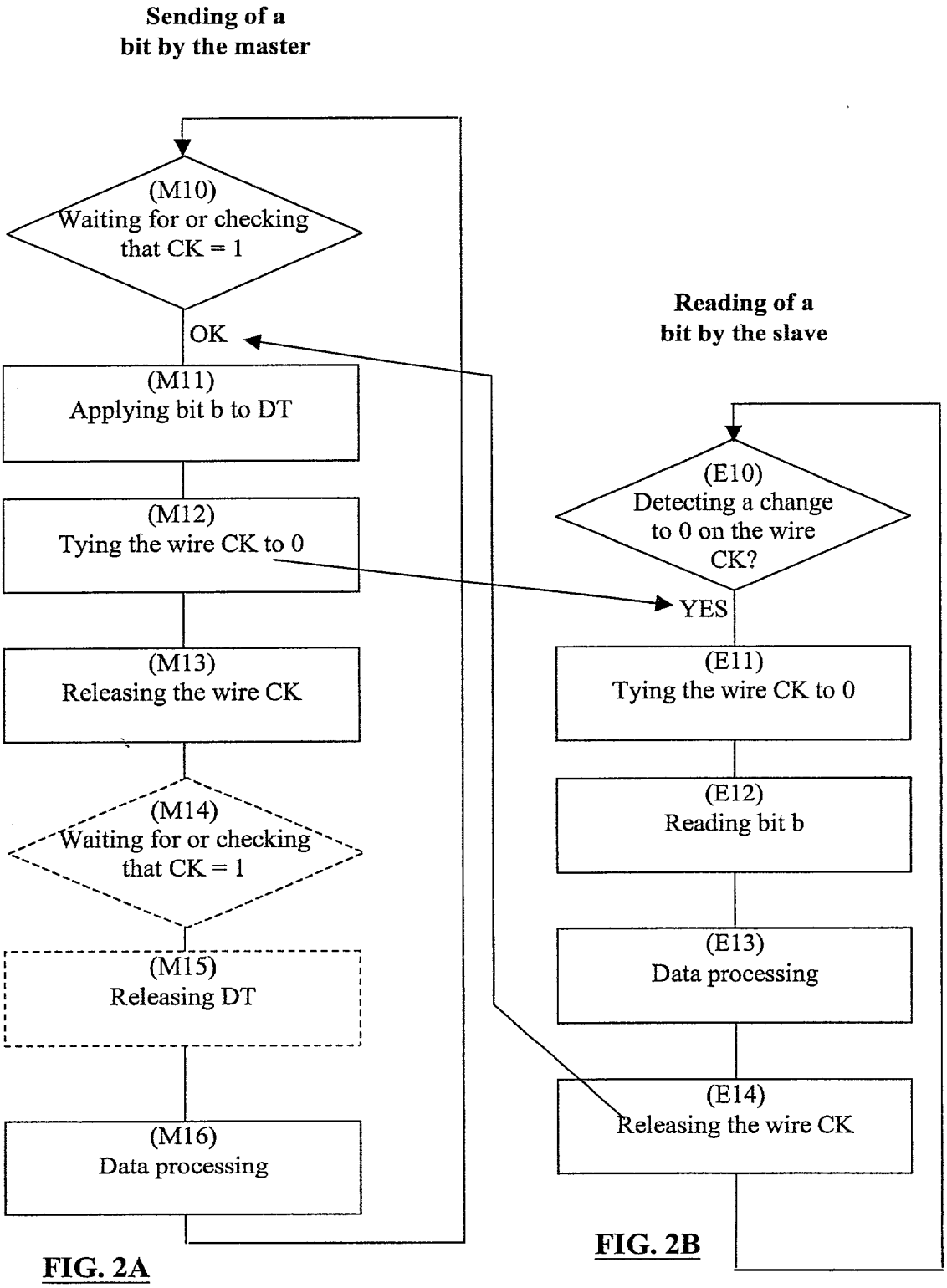


FIG. 2A

FIG. 2B

1002975 - 1101701

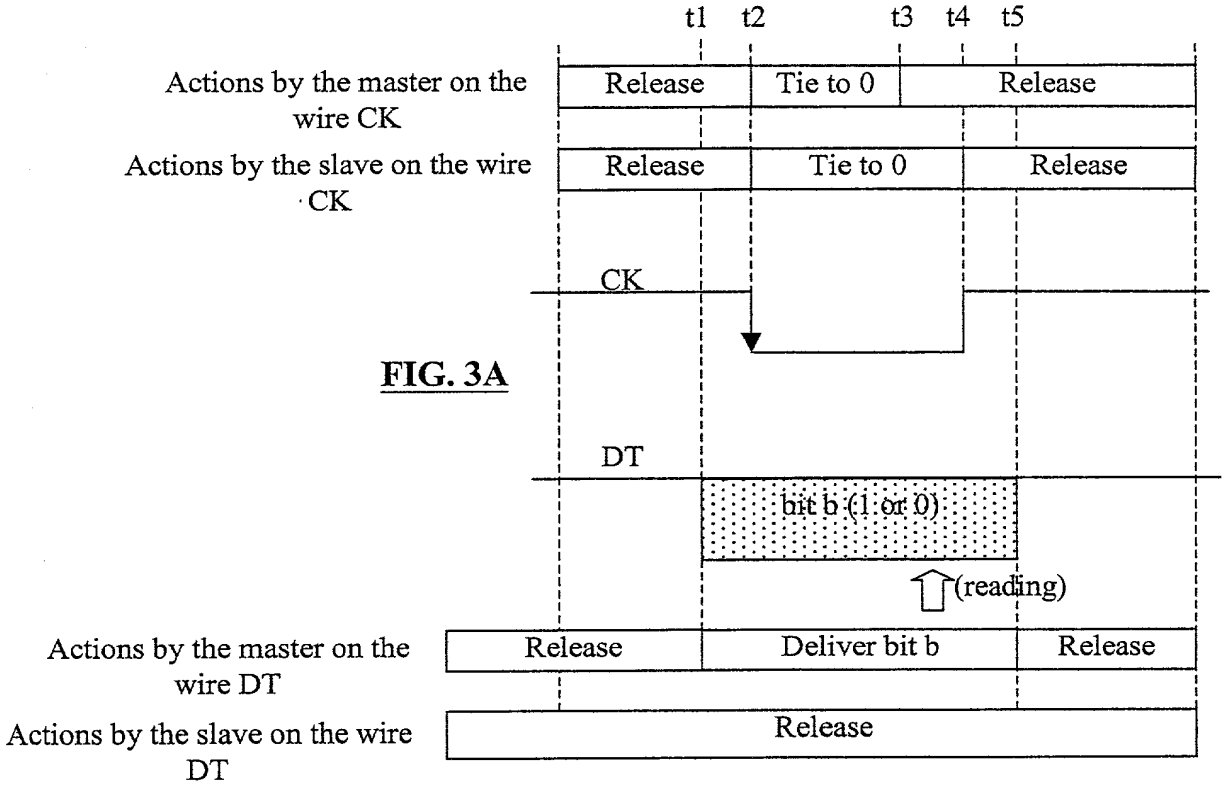


FIG. 3A

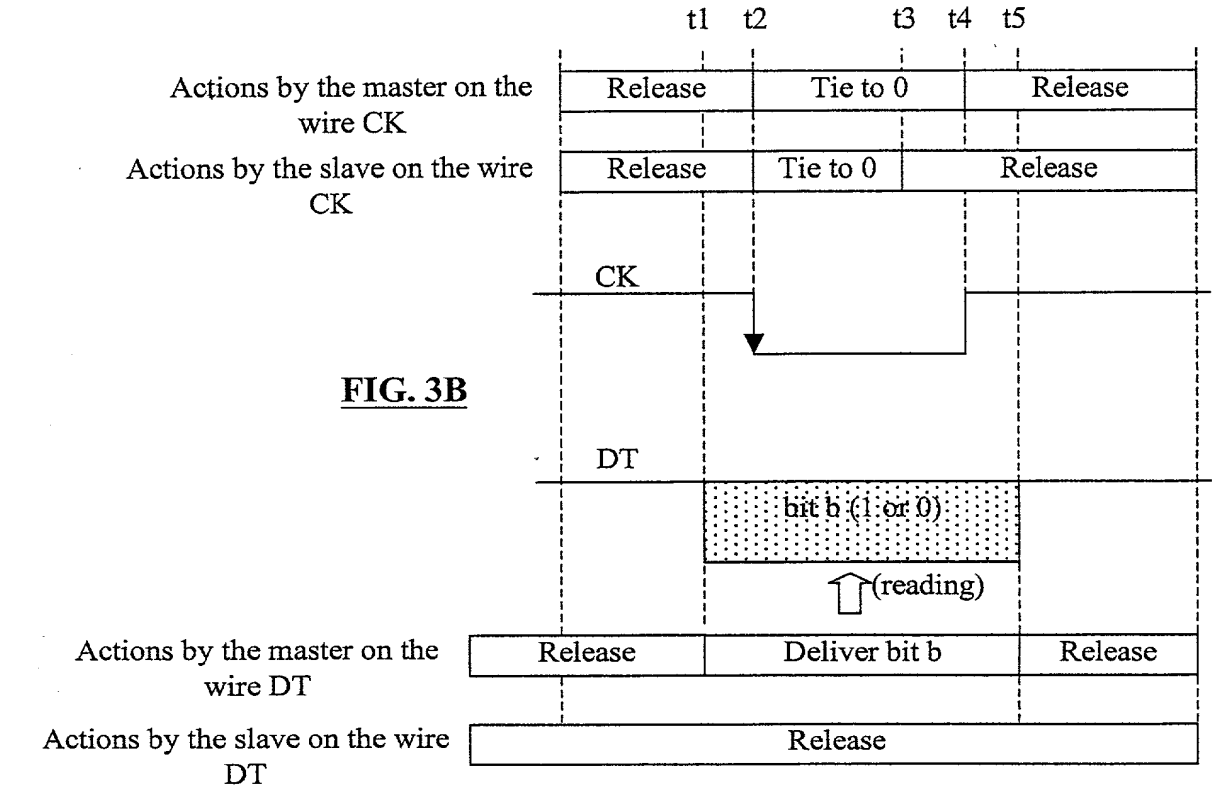


FIG. 3B

FOVOLT-5576.001

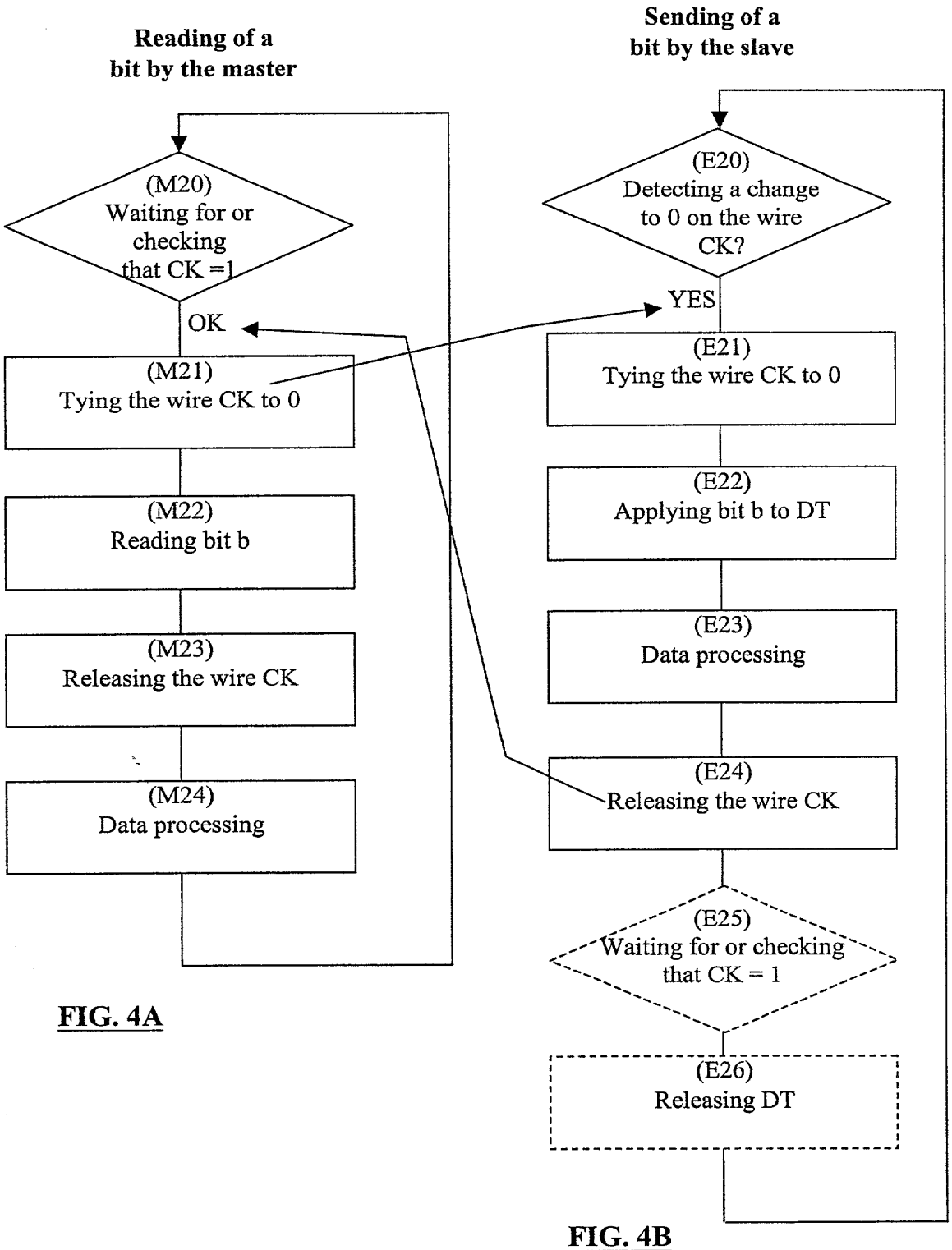

Reading of a bit by the master
(M20) Waiting for or checking that CK =1
OK
(M21) Tying the wire CK to 0
(M22) Reading bit b
(M23) Releasing the wire CK
(M24) Data processing
Sending of a bit by the slave
(E20) Detecting a change to 0 on the wire CK?
YES
(E21) Tying the wire CK to 0
(E22) Applying bit b to DT
(E23) Data processing
(E24) Releasing the wire CK
(E25) Waiting for or checking that CK = 1
(E26) Releasing DT

FIG. 4A

FIG. 4B

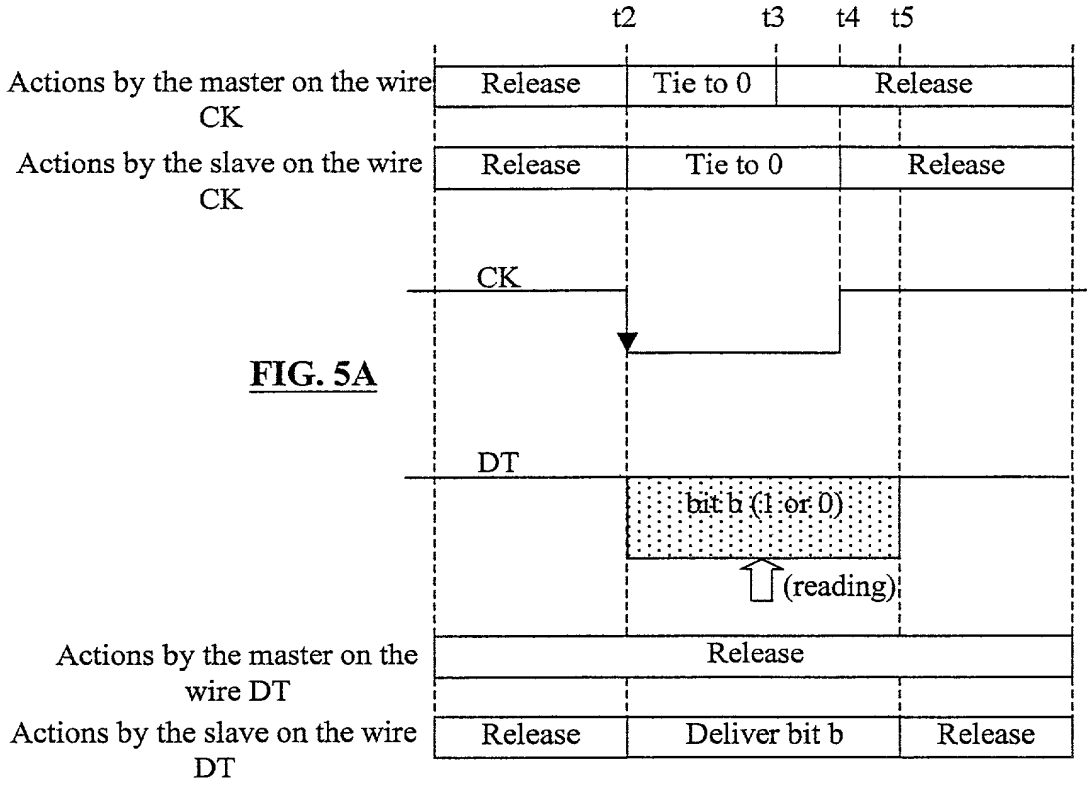

t2
t3
t4
t5
Actions by the master on the wire CK
Release
Tie to 0
Release
Actions by the slave on the wire CK
Release
Tie to 0
Release
CK
DT
bit b (1 or 0)
(reading)
Actions by the master on the wire DT
Release
Actions by the slave on the wire DT
Release
Deliver bit b
Release

FIG. 5A

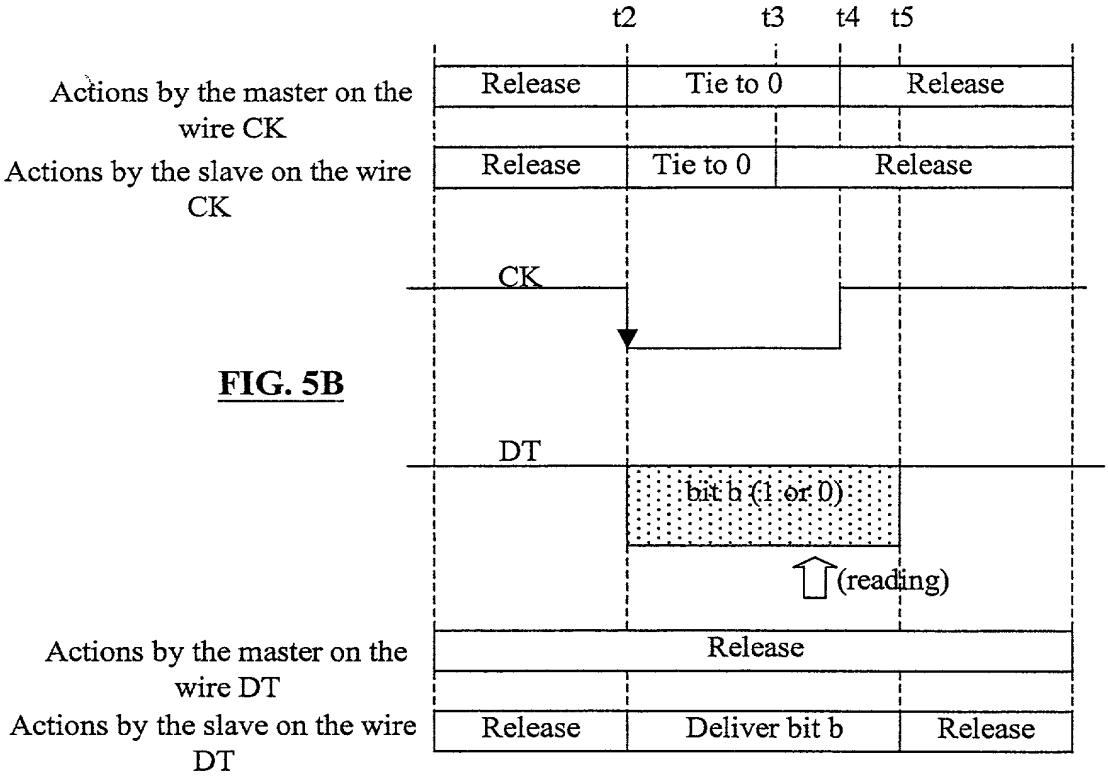
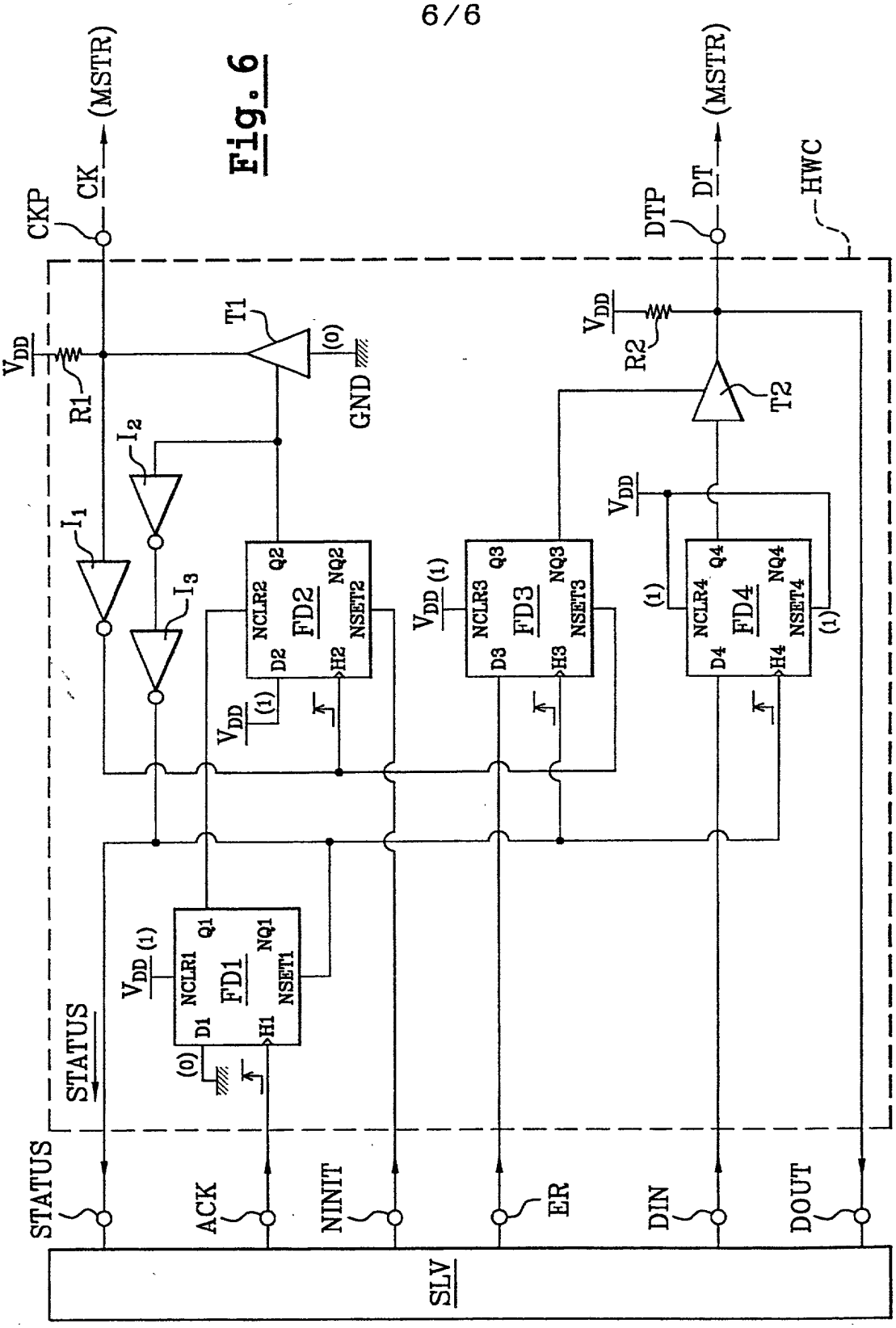

t2
t3
t4
t5
Actions by the master on the wire CK
Release
Tie to 0
Release
Actions by the slave on the wire CK
Release
Tie to 0
Release
CK
DT
bit b (1 or 0)
(reading)
Actions by the master on the wire DT
Release
Actions by the slave on the wire DT
Release
Deliver bit b
Release

FIG. 5B

Fig. 6


CKP
CK
(MSTR)
DTP
DT
(MSTR)
HWC
V_{DD}
R1
T1
(0)
GND
I_1
I_2
I_3
R2
T2
FD1
FD2
FD3
FD4
NCLR1
NCLR2
NCLR3
NCLR4
NSET1
NSET2
NSET3
NSET4
Q1
Q2
Q3
Q4
NQ1
NQ2
NQ3
NQ4
D1
D2
D3
D4
H1
H2
H3
H4
(1)
STATUS
ACK
NINIT
ER
DIN
DOUT
SLV